WHAT IS CLAIMED IS:

1. An image processing apparatus comprising:

a plurality of sensor chips connected to one another, each sensor chip including a first pixel row and a second pixel row, which are formed on the same semiconductor chip, the first pixel row having a plurality of pixels arranged in a main scanning direction, and the second pixel row having a plurality of pixels shifted along the main scanning direction with respect to the first pixel row.

2. An image processing apparatus comprising:

a plurality of sensor chips, each including a first pixel row and a second pixel row, which are formed on the same semiconductor chip, the first pixel row having a plurality of pixels arranged in a main scanning direction, and the second pixel row having a plurality of pixels shifted along the main scanning direction with respect to the first pixel row;

a combining circuit which selectively outputs a signal from the first pixel row and a signal from the second pixel row, wherein said combining circuit is common to said plurality of sensor chips; and

a driving circuit which controls the sequential input of signals from said plurality of sensor chips to said

combining circuit.

3. An image processing apparatus comprising:

a plurality of sensor chips, each including a first pixel row and a second pixel row, which are formed on the same semiconductor chip, the first pixel row having a plurality of pixels arranged in a main scanning direction, and the second pixel row having a plurality of pixels shifted along the main scanning direction with respect to the first pixel row;

a first output line provided outside said plurality of sensor chips, to which a signal from the first pixel row in each of the sensor chips is read;

a second output line provided outside said plurality of sensor chips, to which a signal from the second pixel row in each of the sensor chips is read;

a driving circuit, which drives said plurality of sensor chips to sequentially output signals to the first output line and the second output line; and

a combining circuit provided outside said plurality of sensor chips, which selectively outputs the signals from the first output line and the second output line, wherein said combining circuit is common to said plurality of sensor chips.

4. An image processing apparatus according to Claim 2, further comprising an analog-to-digital converting circuit arranged to receive an output from said combining circuit,

wherein the signals from the first pixel row and the second pixel row are selectively outputted by said combining circuit, and the resulting signal is converted into a digital signal by said analog-to-digital converting circuit.

5. An image processing apparatus according to Claim 3, further comprising an analog-to-digital converting circuit arranged to receive an output from said combining circuit,

wherein the signals from the first pixel row and the second pixel row are selectively outputted by said combining circuit, and the resulting signal is converted into a digital signal by said analog-to-digital converting circuit.

6. An image processing apparatus according to Claim 2, further comprising an analog-to-digital converting circuit,

wherein the signals from the first pixel row and the second pixel row are converted into digital signals by said analog-to-digital converting circuit, and the resulting digital signals are selectively outputted.

7. An image processing apparatus according to Claim 3, further comprising an analog-to-digital converting circuit,

wherein the signals from the first pixel row and the second pixel row are converted into digital signals by said analog-to-digital converting circuit, and the resulting digital signals are selectively outputted.

8. An image processing apparatus according to Claim 2, further comprising:

a first reference level adjusting circuit, which adjusts the reference level of the signal from the first pixel row; and

a second reference level adjusting circuit, which adjusts the reference level of the signal from the second pixel row,

wherein said first reference level adjusting circuit and said second reference level adjusting circuit are provided before said combining circuit.

9. An image processing apparatus according to Claim 3, further comprising:

a first reference level adjusting circuit, which adjusts the reference level of the signal from the first pixel row; and

a second reference level adjusting circuit, which adjusts the reference level of the signal from the second pixel row,

wherein said first reference level adjusting circuit and said second reference level adjusting circuit are provided before said combining circuit.

10. An image processing apparatus comprising:

a plurality of sensor chips, each including an imaging region, a first readout circuit, a second readout circuit, a first output unit, and a second output unit, which are formed on the same semiconductor chip,

the imaging region having a first imaging region and a second imaging region, each having a plurality of pixels arranged in a main scanning direction,

the first readout circuit for selectively reading a signal from the plurality of pixels in the first imaging region,

the second readout circuit for selectively reading a signal from the plurality of pixels in the second imaging region,

the first output unit for outputting the signal read from the first readout circuit, and

the second output unit for outputting the signal read from the second readout circuit;

a combining circuit which selectively outputs the signals from said first output unit and said second output unit, wherein said combining circuit is common to said

plurality of sensor chips; and

a driving circuit, which controls so as to sequentially input the signals from said plurality of sensor chips to said combining circuit.

11. An image processing apparatus comprising:

a plurality of sensor chips, each including an imaging region, a first readout circuit, a second readout circuit, a first output unit, and a second output unit, which are formed on the same semiconductor chip,

the imaging region having a first imaging region and a second imaging region, each having a plurality of pixels arranged in the main scanning direction,

the first readout circuit for selectively reading a signal from the plurality of pixels in the first imaging region,

the second readout circuit for selectively reading a signal from the plurality of pixels in the second imaging region,

the first output unit for outputting the signal read from said first readout circuit, and

the second output unit for outputting the signal read from said second readout circuit;

a first output line provided outside said plurality of sensor chips, to which a signal from the first pixel row in

each of the sensor chips is read;

a second output line provided outside said plurality of sensor chips, to which a signal from the second pixel row in each of the sensor chips is read;

a driving circuit, which drives said plurality of sensor chips to sequentially output signals to the first output line and the second output line; and

a combining circuit provided outside said plurality of sensor chips, which selectively outputs the signals from the first output line and the second output line, wherein said combining circuit is common to said plurality of sensor chips.

12. An image processing apparatus according to Claim 10, further comprising an analog-to-digital converting circuit arranged to receive an output from said combining circuit,

wherein the signals from the first pixel row and the second pixel row are selectively outputted by said combining circuit, and the resulting signal is converted into a digital signal by said analog-to-digital converting circuit.

13. An image processing apparatus according to Claim 11, further comprising an analog-to-digital converting circuit arranged to receive an output of said combining

circuit,

wherein the signals from the first pixel row and the second pixel row are selectively outputted by said combining circuit, and the resulting signal is converted into a digital signal by said analog-to-digital converting circuit.

14. An image processing apparatus according to Claim 10, further comprising an analog-to-digital converting circuit,

wherein the signals from the first pixel row and the second pixel row are converted into digital signals by said analog-to-digital converting circuit, and the resulting digital signals are selectively outputted.

15. An image processing apparatus according to Claim 11, further comprising an analog-to-digital converting circuit,

wherein the signals from the first pixel row and the second pixel row are converted into digital signals by said analog-to-digital converting circuit, and the resulting signals are selectively outputted.

16. An image processing apparatus according to Claim 10, further comprising:

a first reference level adjusting circuit, which

adjusts the reference level of the signal from the first pixel row; and

a second reference level adjusting circuit, which adjusts the reference level of the signal from the second pixel row,

wherein said first reference level adjusting circuit and said second reference level adjusting circuit are provided before said combining circuit.

17. An image processing apparatus according to Claim 11, further comprising:

a first reference level adjusting circuit, which adjusts the reference level of the signal from the first pixel row; and

a second reference level adjusting circuit, which adjusts the reference level of the signal from the second pixel row,

wherein said first reference level adjusting circuit and said second reference level adjusting circuit are provided before said combining circuit.

18. An image processing apparatus according to Claim 1, wherein the second pixel row is shifted by half the pixel pitch in the main scanning direction with respect to the first pixel row.

19. An image processing apparatus according to Claim 1, wherein the first pixel and the last pixel in each of the sensor chips are arranged in different pixel rows.

20. An image processing apparatus according to Claim 1, wherein the number of pixels in the first pixel row is equal to the number of pixels in the second pixel row in each of the sensor chips.

21. An image processing apparatus according to Claim 1, wherein the first pixels in all of the sensor chips are positioned in the same pixel row.

22. An image processing apparatus according to Claim 1, wherein the distance in a sub-scanning direction between the center of the first pixel row and the center of the second pixel row is an integer multiple of the pixel pitch in the main scanning direction.

23. An image processing apparatus according to Claim 1, further comprising:

a light source, which emits light to an original document; and

a lens array, which guides light reflected from the

original document to said plurality of sensor chips.

24. An image processing apparatus according to Claim 2, further comprising:

a light source, which emits light to an original document; and

a lens array, which guides light reflected from the original document to said plurality of sensor chips.

25. An image processing apparatus according to Claim 3, further comprising:

a light source, which emits light to an original document; and

a lens array, which guides light reflected from the original document to said plurality of sensor chips.

26. An image processing apparatus according to Claim 10, further comprising:

a light source, which emits light to an original document; and

a lens array, which guides light reflected from the original document to said plurality of sensor chips.

27. An image processing apparatus according to Claim 11, further comprising:

a light source, which emits light to an original document; and

a lens array, which guides light reflected from the original document to said plurality of sensor chips.